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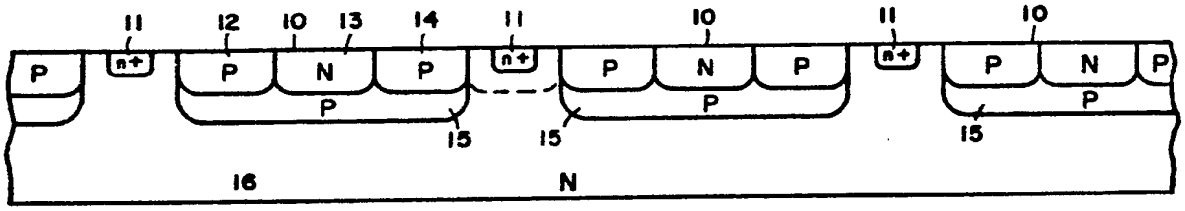

(57) Abstract

A variety of semiconductor devices and technologies can be integrated conveniently using a generic modular substrate (16). The substrate contains modules (10) that can be isolated from each other and from the substrate. This design approach is especially useful for combining high and low voltage functions in the same chip and for integrating analog and digital devices. It is well adapted for CMOS implementations.

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VERSATILE GENERIC CHIP SUBSTRATE

Background of the Invention

There are growing applications for circuits that integrate families of devices, e.g. MOS-bipolar, or diverse functions, e.g. digital-analog, high voltage-low voltage, in the same chip.

Statement of the Invention

We have invented a versatile generic chip substrate that can accommodate a wide variety of device families in a convenient integrated standard array. The substrate contains an intra-isolated array of device sites each of which may contain one or more devices of the variety of device families.

In a preferred embodiment the generic chip substrate is used to form pairs of high voltage and low voltage CMOS devices.

Brief Description of the Drawings

FIGS. 1A-1C are schematic representations of the generic chip substrate (GCS) which comprises the broad aspect of the invention;

FIGS. 2A-2K ("I" omitted) are schematic representations of an exemplary group of devices that can be formed in a selected site of the GCS;

FIG. 3 is a schematic view of a preferred embodiment of the invention showing low voltage and high voltage complementary transistors in a GCS implementation;

FIG. 4 is a schematic representation of a CMOS device integrating digital and analog functions.

Detailed Description

The standard generic chip substrate (GCS) is shown in FIG. 1A and comprises a semiconductor n-substrate 16 with an array of device sites 10 formed as shown. Regions 11 isolate the sites from one another. Each site comprises a sequence of p-n-p tubs 12, 13, 14 formed within a p-well 15. Dimensions of the tubs and doping levels of the various regions are a function of the actual semiconductor

devices to be integrated. A slight variation of the monolithic array illustrated in FIG. 1A would have varying dimensions and doping from site to site with selected sites optimized for a given device family. However the basic ingredients would be common to each site, i.e. n and p tubs in a p-well. (Complementary structures can be used as well.) The sites may be completely isolated from the nearest neighbor as shown schematically in FIG. 1B (plan view) or they can be isolated in groups or rows as indicated in FIG. 1C.

Exemplary of the wide variety of device families that can be accommodated by the GCS are those shown in FIGS. 2A-2K (Legend "21" has been omitted). Other possibilities are possible. The devices in each site have the capability of being totally isolated from other devices in the array. This feature is especially useful when integrating analog and digital devices or high voltage and low voltage devices on the same chip. This layout scheme is shown in plan view in FIG. 1B. Applications will be found in which a series of, for example, low voltage CMOS pairs are advantageously laid out in a row or rows where it is unnecessary to isolate each channel from the others but it is still desirable to isolate the row from other devices, i.e. to isolate the row from the remainder of the chip substrate. In that case the isolating p-well can be formed as a continuous elongated well as shown in FIG. 1C. The basic structure of FIG. 1A is common to either layout.

Referring to FIG. 1A there is shown in dashed lines an n-tub in the separation between the p-wells. While the n-tub in itself provides a degree of isolation, it is often desirable to add the more heavily doped (n^+) region 11 to insure against surface inversion and inter-device leakage. Alternatively, the n^+ region can be used alone and the inter modular spacing optimized for the type and degree of isolation desired.

A high voltage-low voltage CMOS device is shown in FIG. 3. The high voltage device comprises source-substrate

connected structures which are built within p-wells, (11 and 11') across n-tub - p-tub boundaries, utilizing polysilicon as the gate electrodes (12 and 12'). The device structures are as follows:

1) High voltage p-channel: the n-tub region 16 under the polysilicon gate 12 and 2000A gate oxide 13 serves as the inversion region (channel), and the p-tub region 14 under the polysilicon gate 12 and field oxide 15 serves as the drift region. The source and drain are shown at 17 and 18 respectively.

2) n-channel: the p-tub region 16' under the polysilicon gate 12' and 2000A gate oxide 13' serves as the inversion region (channel), and the n-tub region 14' under the polysilicon gate 12' and field oxide 15' serves as the drift region. The source and drain are shown at 17' and 18' respectively.

The portion of the polysilicon gate which runs over the drift region serves as a field plate and insures that the drift region does not become inverted due to stray electric fields. The n^+ and p^+ guard rings 19 and 20 serve as channel stops, i.e. serve to raise the field inversion threshold. Metal contacts are shown at 20. (The gate contacts do not appear in this view.)

3) Low voltage p-channel: the n-tub region 30 under the polysilicon gate 31 provides the channel between source 32 and drain 33.

4) Low voltage n-channel: the p-tub region 30' under the polysilicon gate 31' provides the channel between source 32' and drain 33'. Metal contacts (gate contacts not shown) are denoted 34.

We have fabricated both n- and p-channel HV-CMOS devices with drain to source breakdown voltages greater than 100 volts. Device characteristics are presented in the following Table. Devices had these dimensions:

width = 200 μm, length = 15 μm, drift region 10 μm. Additional details on device structure and fabrication appear in IEEE Journal of Solid-State Circuits, E. Habekotte, B. Hoefflinger, W. Renker, and G. Zimmer, Vol. SC-16, No. 3, June, 1981. R_{ON} in the Table is on-resistance measured with V_{GS}=10V and V_{DS}-1V. C_{GD} in the Table is the gate/drain overlap capacitance.

HV CMOS Device Characteristics

R_{ON} (HV-NCH)	1.08k Ω
R_{ON} (HV-PCH)	10.1k Ω
C_{GD}	7.67×10^{-14} F
C_{GD}/Width	3.84×10^{-16} F/μm of width

The addition of a p-well to the CMOS process affords a variety of additional design capabilities. For example:

1) Low voltage p-channel devices can be fabricated in n-tubs contained within a p-well (FIG. 2B), thus providing individually isolated p-channel devices.

2) Low voltage digital circuits can be fabricated in one large p-well (FIG. 4), thus providing a vehicle for isolating analog and digital portions of a circuit.

3) Complementary bipolar transistors (npn and pnp) can be fabricated within the p-well (FIG. 2H). These devices are also individually isolated from each other and the substrate.

4) If one utilizes the substrate, a controlled pnpn SCR is also available (FIG. 2H).

Claim

An integrated semiconductor structure comprising a semiconductor substrate (16) of a first conductivity type having a plurality of repeating cell units,

CHARACTERIZED IN THAT

each unit comprises a relatively deep well (15) having a second conductivity type opposite to that of the substrate, each said well contains at least three contiguous tubs (12, 13, 14) of alternating conductivity type, isolating means (11) between at least selected wells for electrically isolating those wells from each other, and at least one p-n junction device (e.g., FIG. 3) formed in at least one of said tubs.

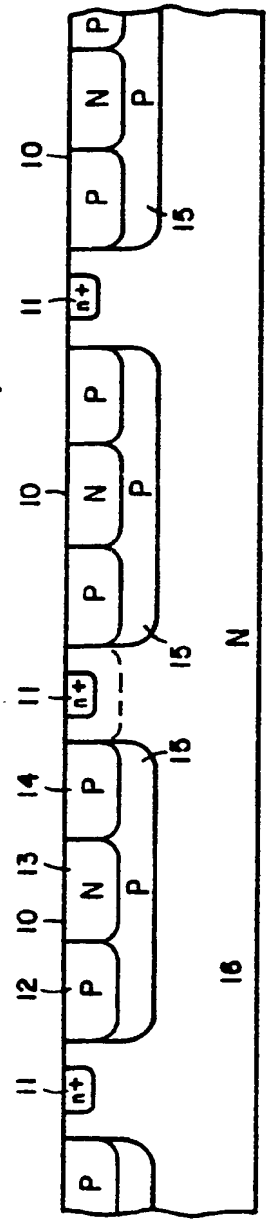

FIG. 1A

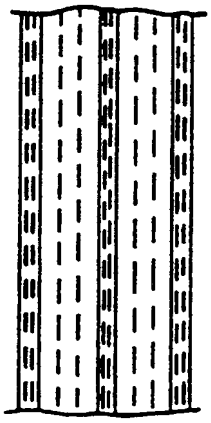

FIG. 1C

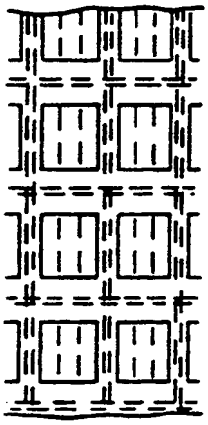

FIG. 1B

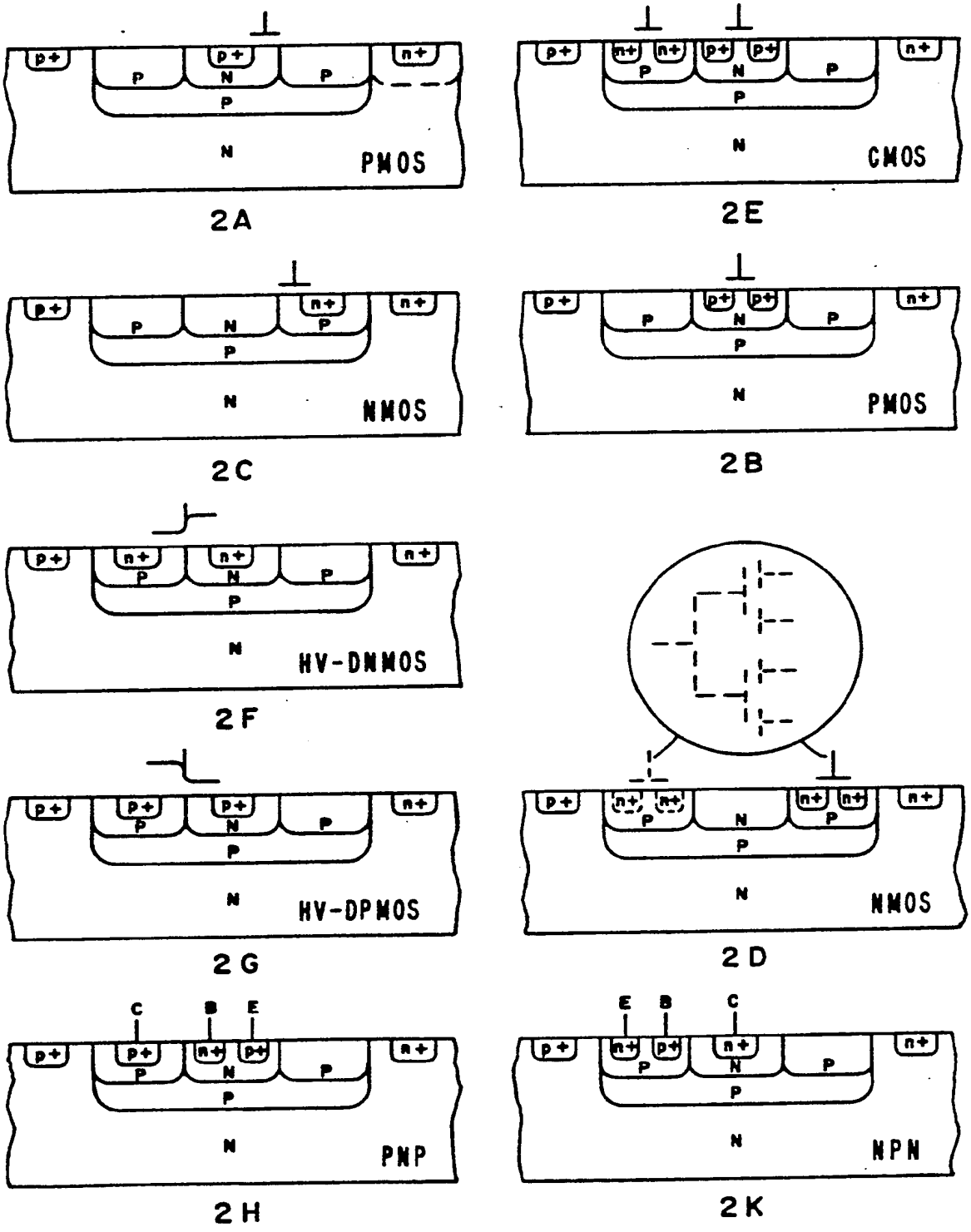
PMOS
2A
CMOS
2E
NMOS
2C
PMOS
2B
HV-DNMOS
2F
NMOS
2D
HV-DPMOS
2G
PNP
C B E
2H
NPN
E B C
2K

FIG. 2

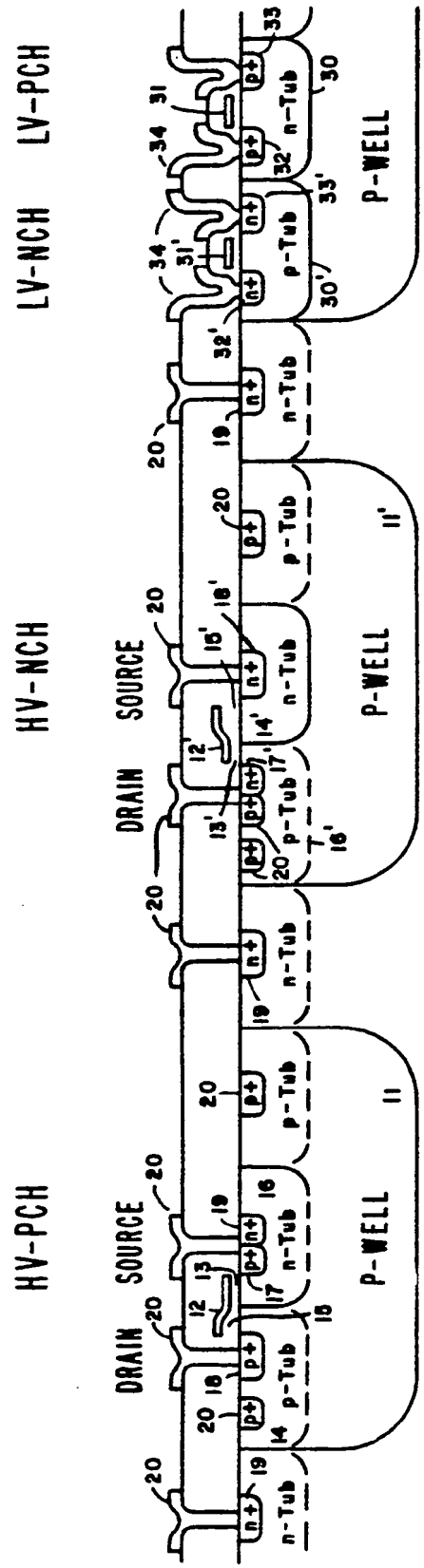
HV-PCH
HV-NCH
LV-NCH
LV-PCH
DRAIN
SOURCE
P-WELL
n-Tub
p-Tub
n⁻ epi
n⁺ SUBSTRATE

FIG. 3

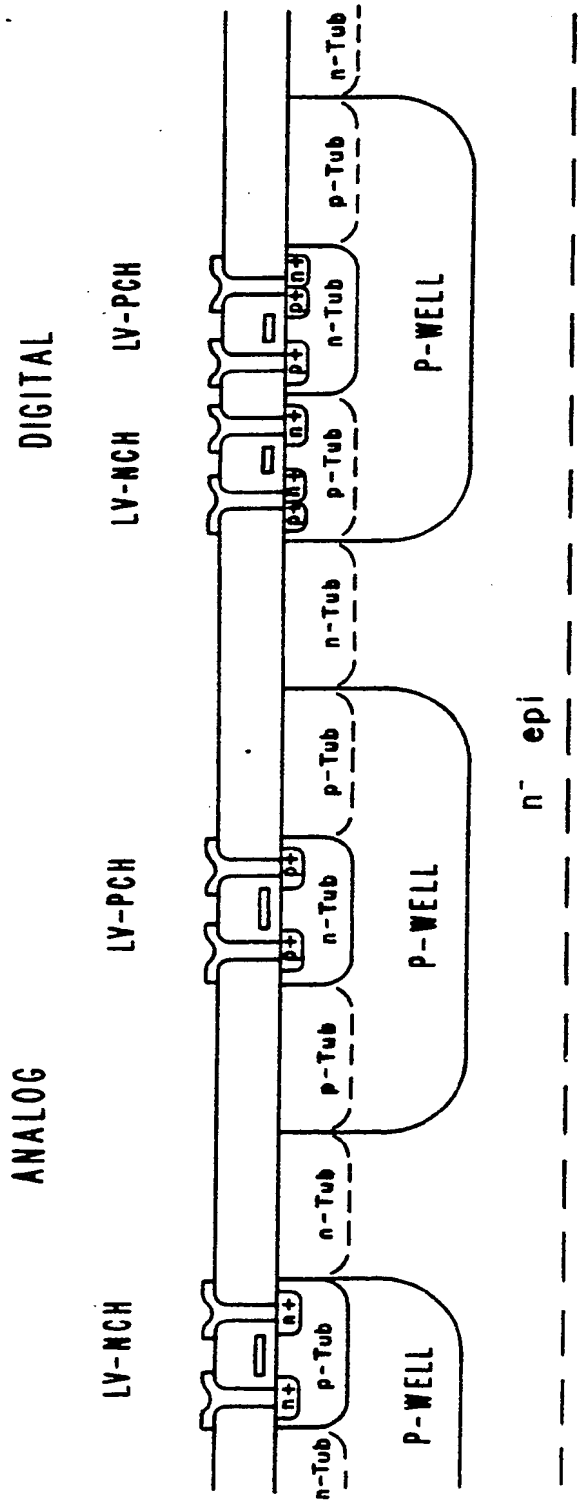
ANALOG
DIGITAL
LV-NCH
LV-PCH
LV-NCH
LV-PCH
n-Tub
p-Tub
P-WELL
n⁻ epi
n⁺ SUBSTRATE

FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 85/00262

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 27/06; H 01 L 21/76

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	Patents Abstracts of Japan, vol. 8, no. 25 (E-225)(1462), 2 February 1984 & JP, A, 58188152 (Nippon Denki K.K.) 2 November 1983, see abstract and figures	1
A	IEEE Journal of Solid-State Circuits, vol. SC-18, no. 3, June 1983 (New York, US) B.T. Murphy: "Micro-computers: trends, technologies and design strategies", pages 236-244, see page 238, figures 4-5, column 2	1
A	US, A, 4403395 (P.A. CURRAN) 13 September 1983 see figure 12; column 1, lines 1-37	1
A	IEEE Journal of Solid-State Circuits, vol. SC-16, no. 3, June 1981 (New York, US) E. Habekotté et al.: "A coplanar CMOS power switch", pages 212-226, see figure 17 (cited in the application)	1

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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
13th May 1985	13 JUIN 1985
International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

Form PCT/ISA/210 (second sheet) (January 1985)

1

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	Patents Abstracts of Japan, vol. 7, no. 99 (E-172)(1244), 27 April 1983 & JP, A, 5821857 (Suwa Seikosha K.K.) 8 February 1983; see abstract and figures	1

Form PCT ISA/210 (extra sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 8500262 (SA 8981)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 06/06/85

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 4403395	13/09/83	FR-A,B	2449334	12/09/80
		DE-A-	3005384	28/08/80
		NL-A-	8000665	19/08/80
		JP-A-	55146944	15/11/80
		US-A-	4325180	20/04/82

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